In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Original) A compressor of a multiplier comprising:

a first compressor, wherein said first compressor comprises:

a first plurality of inputs;

a summation output;

a first carry bit output; and

a first plurality of transistor paths connecting each of said first plurality of inputs to said summation output, wherein a first compressor critical transistor stage path level within said first compressor is less than seven; and

a successive compressor, wherein said successive compressor comprises:

a second plurality of inputs; and

a plurality of successive transistor paths connecting at least one of said first plurality of inputs to said first carry bit output and connecting said first carry bit output to at least one of said second plurality of inputs, wherein a successive compressor critical transistor stage path level within said successive compressor is less than eight.

2. (Original) The compressor of claim 1, wherein said first compressor further comprises:

a second carry bit output; and

a second plurality of transistor paths connecting each of said first plurality of inputs to said second carry bit output.

3. (Original) The compressor of claim 2, wherein each of said first plurality of transistor paths, each of said second plurality of transistor paths, and each of said plurality of successive

transistor paths comprises a plurality of switches and a plurality of inverters.

4. (Original) The compressor of claim 3, wherein said switches and said inverters form a plurality of logic stages for each of said first plurality of inputs.

5. (Original) The compressor of claim 4, wherein at least one of said logic stages for at least one of said first plurality of inputs is a transfer gate XOR stage and at least one of said logic stages for at least one of said first plurality of inputs is a transfer gate XNOR stage.

6. (Original) The compressor of claim 3, wherein when one of said first plurality of inputs is connected to a source of one said switches, said input is not connected to a gate of another of said switches, and when one of said first plurality of inputs is connected to a gate of one said switches, said input is not connected to a source of another of said switches.

7. (Original) The compressor of claim 3, wherein a drain of each of said switches is not connected to a source of another of said switches.

8. (Original) The compressor of claim 4, wherein when one of said inverters within one of said logic stages is connected to a source of one of said switches within the same logic stage as said inverter, said inverter is not connected to a gate of another of said switches within the same logic stage as said inverter, and when one of said inverters within one of said logic stages is connected to a gate of one of said switches within the same logic stage as said inverter, said inverter is not connected to a source

of another of said switches within the same logic stage as said inverter.

9. (Original) The compressor of claim 4, wherein a first compressor critical logic stage path level is three within said first compressor and a successive compressor critical logic stage path level is three within said successive compressor.

10. (Original) The compressor of claim 2, wherein said first compressor critical transistor stage path level within said first compressor is six and said successive compressor critical transistor stage path level within said successive compressor is seven.

11. (Original) The compressor of claim 10, wherein a number of said first plurality of inputs is five.

12. (Original) The compressor of claim 4, wherein a first compressor critical logic stage path level is less than four and a successive compressor critical logic stage path level is less than four.

13. (Original) The compressor of claim 2, wherein a number of binary ones in the first plurality of inputs is the sum of two times the first carry bit output, two times the second carry bit output, and the summation output.

14. (Original) The compressor of claim 13, wherein the summation output, the second carry bit output, and the first carry bit output, are logically expressed as

$So = ((Bi \oplus Ci) \oplus (Di \oplus Ai)) \oplus Xi;$

$Co = ((Bi \oplus Ci) \oplus (Di \oplus Ai)) \cdot Xi + \overline{((Bi \oplus Ci) \oplus (Di \oplus Ai))} \cdot Ai;$ and

$Xo = (Bi \oplus Ci) \cdot Di + \overline{(Bi \oplus Ci)} \cdot Bi.$

Claims 15 to 26. (Canceled)

27. (Original) A compressor of a multiplier comprising:

a first compressor, wherein said first compressor comprises:

a first plurality of inputs;

a summation output;

a first carry bit output;

a first plurality of transistor paths comprising a plurality of switches and a plurality of inverters connecting each of said first plurality of inputs to said summation output;

a second carry bit output; and

a second plurality of transistor paths comprising a plurality of switches and a plurality of inverters connecting each of said first plurality of inputs to said second carry bit output, wherein when one of said first plurality of inputs is connected to a source of one said switches, said input is not connected to a gate of another of said switches, and when one of said first plurality of inputs is connected to a gate of one said switches, said input is not connected to a source of another of said switches.

28. (Original) The compressor of claim 27, further comprising:

a successive compressor, wherein said successive compressor comprises:

a second plurality of inputs; and

a plurality of successive transistor paths connecting at least one of said first plurality of inputs to said first carry bit output and connecting said first carry bit output to at least one of said second plurality of inputs.

29. (Original) A compressor of a multiplier comprising:

a first plurality of inputs;

a summation output;

a first carry bit output;

a first plurality of transistor paths connecting each of said first plurality of inputs to said summation output;

a second carry bit output; and

a second plurality of transistor paths connecting each of said first plurality of inputs to said second carry bit output, wherein each of said second plurality of transistor paths comprises a plurality of switches and a plurality of inverters, wherein a drain of each of said switches is not connected to a source of another of said switches.

30. (Original) The compressor of claim 29, further comprising:

a successive compressor, wherein said successive compressor comprises:

a second plurality of inputs; and

a plurality of successive transistor paths connecting at least one of said first plurality of inputs to said first carry bit output and connecting said first carry bit output to at least one of said second plurality of inputs.

31. (Original) A compressor of a multiplier comprising:

a first compressor, wherein said first compressor comprises:

a first plurality of inputs;

a summation output;

a first carry bit output;

a first plurality of transistor paths connecting each of said first plurality of inputs to said summation output;

a second carry bit output; and

a second plurality of transistor paths connecting each of said first plurality of inputs to said second carry bit output, wherein each of said first plurality of transistor paths and each of said second plurality of transistor paths comprises a plurality of switches and a plurality of inverters and said switches and said inverters form a plurality of logic stages for each of said first plurality of inputs and said at least one carry bit input, wherein when one of said inverters within one of said logic stages is connected to a source of one of said switches within the same logic stage as said inverter, said inverter is not connected to a gate of another of said switches within the same logic stage as said inverter, and when one of said inverters within one of said logic stages is connected to a gate of one of said switches within the same logic stage as said inverter, said inverter is not connected to a source of another of said switches within the same logic stage as said inverter.

32. (Original) The compressor of claim 31, further comprising:

a successive compressor, wherein said successive compressor comprises:

a second plurality of inputs; and

plurality of successive transistor paths connecting at least one of said first plurality of inputs to said first carry bit output and connecting said first carry bit output to at least one of said second plurality of inputs.

33. (Original) A compressor of a multiplier comprising:

a first compressor, wherein said first compressor comprises:

a first plurality of inputs;

a first carry bit output;

a second carry bit output; and

a first plurality of transistor paths connecting each of said first plurality of inputs to said second carry bit output, wherein a first compressor critical transistor stage path level within said first compressor is less than seven; and

a successive compressor, wherein said successive compressor comprises:

a second plurality of inputs; and

a plurality of successive transistor paths connecting at least one of said first plurality of inputs to said first carry bit output and connecting said first carry bit output to at least one of said second plurality of inputs, wherein a successive compressor critical transistor stage path level within said successive compressor is less than eight.

34. (Original) The compressor of claim 33, wherein each of said first plurality of transistor paths and each of said plurality of successive transistor paths comprises a plurality of switches and a plurality of inverters and said switches and said inverters form a plurality of logic stages for each of said first plurality of inputs, wherein a first compressor critical logic stage path level is less than four and a successive compressor critical logic stage path level is less than four.

Claims 35 and 36. (Canceled)